REMARKS

Claims 1-40 are pending in this application, of which claim 4 has been withdrawn from consideration and claims 15, 22, 26, 28-37 and 40 have been amended. No new claims have been added.

A substitute specification is attached hereto correcting various grammatical, idiomatic and spelling errors. No new matter has been added.

The Examiner has objected to claims 30-37 and 40 for an informality which has been corrected in the aforementioned amendments.

Claims 15 and 26 stand rejected under 35 USC §112, first paragraph, for failing to comply with the enablement requirement.

Accordingly, claims 15 and 26 have been amended to address this rejection, which should be withdrawn.

Claims 15, 22-23, 26 and 28-30 stand rejected under 35 USC §112, second paragraph, as indefinite.

Accordingly, claims 15, 22, 26 and 28-30 have been amended to correct the noted instances of indefiniteness, and the 35 USC §112, second paragraph, rejection should be withdrawn.

Claims 1-3, 5, 8 and 10-27 stand rejected under 35 USC §103(a) as unpatentable over U.S. Patent 5,441,012 to Tsukiji et al. (hereinafter "**Tsukiji et al.**") in view of Adachi et al., "Chemical

Etching of InGaAsP/InP DH Wafer", 1046 Journal of Electrochemical Society, Vol. 129 (1982) (hereinafter "**Adachi et al.**").

Applicants respectfully traverse this rejection.

Tsukiji et al. discloses a method of manufacturing a laser diode. The method includes the steps of forming a mesa on a p-type compound semiconductor substrate 1 by sequentially arranging at least a p-type compound semiconductor cladding layer 2, an active layer 3 and an n-type compound semiconductor compound layer 4, burying the lateral sides of said mesa with a p-type compound semiconductor buried layer 6 and an n-type compound semiconductor current blocking layer 7, removing said n-type compound semiconductor current blocking layer 7 partly at areas contacting each of the lateral sides of said mesa to partly expose the p-type compound semiconductor buried layer 6 in the vicinity of said mesa and then burying the remaining space with a p-type compound semiconductor current blocking layer 8.

The Examiner has admitted that **Tsukiji et al.** fails to disclose that the InP layer is etched by an etchant including hydrochloric acid and acetic acid, but has cited **Adachi et al.** for teaching this feature.

Applicants respectfully disagree.

Adachi et al. discloses a mesa structure formed by etching InGaAsP/InP double heterostructure (DH) by using a plurality of kinds of etchants.

On the other hand, an object of the present invention is to flatten a convex structure formed by crystal growth, which is totally distinct from the teachings of **Adachi et al.**, which disclose forming the mesa structure.

Therefore, one of ordinary skill in the art would not use the etchant used in **Adachi et al.** for flattening the convex structure formed by crystal growth. Hence, one of ordinary skill in the art would not apply the teachings of **Adachi et al.** to the teachings of **Tsukiji et al.** whereby the convex structure formed by crystal growth is flattened. In addition, there is no motivation and suggestion to combine the teachings of **Adachi et al.** and **Tsukiji et al.**

Thus, the 35 USC §103(a) rejection should be withdrawn.

Claims 6-7 stand rejected under 35 USC §103(a) as unpatentable over **Tsukiji et al.** in view of **Adachi et al.** and further in view of U.S. Patent 6,037,189 to Goto (hereinafter "**Goto**").

Applicants respectfully traverse this rejection.

Goto has been cited for teaching that the InP layer is flat and has at least one of (or is closer to) a (100) surface, a (011) surface, or a (0-1-1) surface, but like the other cited references, fails to teach, mention or suggest the limitations recited in claim 1, from which these claims depend.

Thus, the 35 USC §103(a) rejection should be withdrawn.

Claim 9 stands rejected under 35 USC §103(a) as unpatentable over **Tsukiji et al.** in view of **Adachi et al.** and further in view of Kimura et al. (hereinafter "**Kimura et al.**").

Applicants respectfully traverse this rejection.

Kimura et al. has been cited for teaching the InP layer (17) has flat surface located at a height corresponding to a highest position of the surface of the starting growth (Fig. 6d).

Like the other cited references, **Kimura et al.** fails to teach, mention or suggest the limitations recited in claim 1, from which claim 9 depends, and the 35 USC §103(a) rejection should be withdrawn.

Claims 38-39 stand rejected under 35 USC §103(a) as unpatentable over **Kimura et al.** in view of U.S. Patent 6,110,576 to Otsuka et al. (hereinafter "**Otsuka et al.**") and **Adachi et al**.

Applicants respectfully traverse this rejection.

Kimura et al., in Fig. 8(c), discloses the three semiconductor layers arranged as recited in claim 38, but fails to teach, mention or suggest that the bandgap of the second semiconductor layer is smaller than the bandgap of InP on the first semiconductor layer, but the Examiner has cited **Otsuka et al.** for teaching this feature.

As discussed above, the enchant disclosed in **Adachi et al**. is used for forming the mesa structure. Hence, one of ordinary skill in the art would not use the etchant used in **Adachi et al**. for flattening the convex structure formed by crystal growth. Therefore, one of ordinary sill in the art would not apply the technology disclosed in **Adachi et al**. to the teachings of either **Kimura et al.** or **Otsuka et al.** to teach the present invention.

Thus, the 35 USC §103(a) rejection should be withdrawn.

The Examiner has indicated that claims 28-30 would be allowable if rewritten to correct typographical errors, and the 35 USC §112, second paragraph, rejection, and that claims 31-37 and 40 would be allowable if rewritten to correct typographical errors.

Accordingly, claims 28-30 and 31-37 have been amended to correct these typographical errors.

In view of the aforementioned amendments and accompanying remarks, claims 1-3 and 5-40, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Substitute Specification w/marked-up version

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